9. Old Question Papers

Code No: 133AJ **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, April/May - 2018
DIGITAL LOGIC DESIGN
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Convert $(67A9)_{16}$ into decimal.	[2]
b)	Add (+80) and (-70) using 2's complement.	[3]
c)	Write the truth table of Ex-OR Gate.	[2]
d)	Implement OR gate using NAND gates only.	[3]
e)	Write the truth table of half adder.	[2]
f)	Design half sub tractor circuit.	[3]
g)	Differentiate between Latch and flip flop.	[2]
h)	Draw the circuit diagram of Ring counter.	[3]
i)	Differentiate between RAM and ROM.	[2]
j)	Name any 3 logic micro operations.	[3]

PART-B

(50 Marks)

2.a) i) Convert $(657)_8$ into decimal.
ii) Convert $(2348)_{10}$ into hexa decimal.
b) Represent the decimal number 46.5 as a floating point number with 16 bit mantissa and 8 bit exponent. [5+5]

OR

3.a) i) Convert 110001.1010010 into hexadecimal.
ii) Convert $(423.25)_{10}$ into Hex.
b) i) Simplify A(B+C)+AB+ABC
ii) Write the truth table and symbols of AND and OR gates. [5+5]

4. Obtain the simplified expression in sum of products for the following Boolean function.
a) $F(A,B,C,D) = \sum(2,3,12,13,14,15)$.
b) $BDE+B'C'D+CDE+A'B'CE+A'B'C+B'C'D'E'$ [5+5]

OR

5. Obtain the simplified expression in product of sums.
a) $F(A,B,C,D) = \pi(0,1,2,3,4,10,11)$
b) $F(A,B,C,D) = \pi(1,3,5,7,13,15)$ [5+5]

6.a) Design half adder using only NAND gates.
b) Design a combinational circuit which converts BCD to Excess-3 code. [5+5]

OR

7.a) Design a 2 bit magnitude comparator.
b) Implement 4*16 decoder using two 3*8 decoders. [5+5]

8.a) Explain a right shift register.
b) Design a 3 bit Ripple counter. [5+5]

OR

9.a) What is a hazard? How do you eliminate hazards?
b) Design and explain Johnson counter. [5+5]

10.a) Explain different types ROMs.
b) Implement the following Boolean functions using PLA with 3 AND gates.
F_1 (ABC) = $\sum$ (3,5,7), $F_2 = \sum(4,5,7)$. [5+5]

OR

11.a) Explain the applications of Logic micro operations.
b) Explain shift Right and Left with examples. [5+5]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, May/June - 2019
DIGITAL LOGIC DESIGN
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
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PART- A

(25 Marks)

1.a) What are 2's complement and 9's complement of a numbers? Give examples. [2]
b) State and prove De Morgan theorems. [3]
c) What are minterms and maxterms? Give examples for each. [2]
d) Define pair quad and octet in K-Maps and give examples. [3]
e) Draw the logic circuit of a full adder and give its truth table. [2]
f) Write the functions of a decoder and multiplexer. [3]
g) Draw the logic diagram of a master slave J-K flip-flop. [2]
h) Describe the race free state assignment in asynchronous sequential circuits. [3]
i) What are PLAs and PALs? [2]
j) Explain about arithmetic operations with examples. [3]

PART-B

(50 Marks)

2.a) Explain various number systems and codes and their conversion with examples for each.
b) Simplify the following Boolean expressions to a minimum number of literals
(i) ABC+A'B+ABC' (ii) xy + x(wz+wz') [5+5]

OR

3.a) Express the following numbers in decimal : $(10110.0101)_2$, $(16.5)_{16}$, $(26.24)_8$.
b) Demonstrate by means of truth tables the Boolean Associative law and distributive law.
c) Simplify the Boolean expression to minimum number of literals: (A+B)' (A'+B'). [10]

4.a) Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates
$F(A,B,C,D) = \sum 0,2,4,5,6,7,8,10,13,15)$
b) Show that the dual of the exclusive OR is also its compliment. [5+5]

OR

5.a) Draw the multiple level NAND circuit for the following expression:
$(AB'+CD')E + BC(A+B)$
b) Simplify the following four variable Boolean function and implement the same using NAND logic. F (A, B, C, D) = $\sum$ (0, 2, 4, 5, 6, 7, 8, 10, 13, 15) [5+5]

6.a) Construct a 4-bit BCD adder-substractor circuit using BCD adder and 9's complementer.

b) Explain the working and functions of decoders and encoders. Construct 2/4 line decoder with logic gates with enable input. [5+5]

OR

7.a) Construct a 4 bit 2's complement adder using full adders and perform addition and subtraction by taking 4-bit numbers with examples.

b) Explain the design procedure for multiplexers and de-multiplexers and draw the logic diagram of a 4-to-1 line multiplexer with logic gates. [5+5]

8.a) Design 4-bit shift register using D flip-flops and explain its working with the help of timing diagrams.

b) Design a counter with the following repeated binary sequence: 0,1,2,3,4,5,6, use JK flip-flops. [5+5]

OR

9.a) Draw the circuit diagram of a 4-bit binary counter with parallel load and explain its working with its function table.

b) Design a 4 bit synchronous counter with D flip - flops and explain its working. [5+5]

10.a) Given 32 × 8 ROM with enable input, Show the external connections necessary to construct a 128 × 8 ROM with 4 chips and a decoder.

b) Explain the working of a PLA with a schematic and implement the following two Boolean functions with a PLA:
$F_1 (A, B, C) = \sum (0, 1, 2, 4)$ and $F_2 (A,B,C) = \sum (0.5.6.7)$. [5+5]

OR

11.a) Explain the functions and applications of PLAs in memory addressing and implement the following two Boolean functions with a PLA:
$F_1 (A, B, C) = \sum (0, 1, 3, 5)$ and $F_2 (A, B, C) = \sum (1, 2, 4, 7)$

b) What are sequential programmable devices? Draw the sequential programmable logic for a basic microcell logic. [5+5]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, November/December - 2017
DIGITAL LOGIC DESIGN
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

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Part A is compulsory which carries 25 marks. Answer all questions in Part A.
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PART- A

(25 Marks)

1.a) Subtract the following using 1's and 2's complement $(101)_2$ - $(10110)_2$. [2]
b) Distinguish between canonical and standard forms by giving an example. [3]
c) Derive the sum of minterms for the function f(a,b,c)=a′b+b′c′ [2]
d) Implement the following function using only NAND Gates F=a.(b′+ c′) + (b. c). [3]
e) Differentiate multiplexer and de-multiplexer. [2]
f) Draw the diagram of 4-Bit Parallel adder cum parallel subtractor. [3]
g) Show the excitation table and truth table of JK flip flop. [2]
h) Differentiate critical and non-critical race. [3]
i) Define Register Transfer Language. [2]
j) Differentiate PLA and PAL. [3]

PART-B

(50 Marks)

2.a) What are the various logic gates, give the representation along with the truth table.
b) What is the use of complements? Perform subtraction using 7's complement for the given Base-7 numbers (565)-(666). [5+5]

OR

3.a) Convert the following to the corresponding bases
i) $(9BCD)_{16}$ = ( )$_8$
ii) $(323)_4$ = ( )$_5$
b) Given the 8 bit data word 11011011, generate the 12 bit composite word for the Hamming code that corrects and detects single errors. [5+5]

4.a) Derive the product of maxterms for f(a,b,c,d)=a.b.c+ b′.d+c.d′.
b) Derive and Implement Exclusive OR function involving three variables using only NAND function. [5+5]

OR

5.a) Obtain the simplified expression in SOP form of F(a,b,c,d,e)=$\sum$(1,2,4,7,12,14,15,24,27,29,30,31)using K-maps.
b) Implement the function f(a,b,c)=π(0,1,3,4) using NAND-NAND two level gate structure. [5+5]

6.a) Implement and odd parity generator for 3-bit using a decoder.

b) Design a circuit for 2-bit binary multiplier. [5+5]

OR

7.a) Define a multiplexer? Draw a 4:1 multiplexer for the function
$f(a,b,c,d)=\sum(0, 4,5,10,11,12,15)$

b) Design a full binary adder with two half adders and a OR gate. [5+5]

8.a) Explain about a NOR Latch in detail, with a neat diagram.

b) Design a 3-bit counter using T flip flops. [5+5]

OR

9. Define essential hazard? Implement SR Latch by avoiding Hazard Neatly draw the diagram of SR latch before hazard and after Hazard elimination. [10]

10. Explain about RAM in detail. [10]

OR

11. What is a micro operation? List and explain its categories with relevant examples. [10]

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Part A is compulsory which carries 25 marks. Answer all questions in Part A.
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PART- A

(25 Marks)

1.a) Write the advantages of floating-point representation. [2]
b) Distinguish between weighted and non-weighted codes with example. [3]
c) What is the use of don't care combinations? [2]
d) Implement the following function using only NOR Gates F=a.(b+ c) + (b. c). [3]
e) Define a combinational circuit , give its block diagram. [2]
f) Write a short notes on priority encoder. [3]
g) Differentiate between a latch and a flip flop. [2]
h) Define Hazard. Mention various types of hazards. [3]
i) Why programmable AND gates are used in PLA instead of a decoder. [2]
j) Write the applications of logical micro operations. [3]

PART-B

(50 Marks)

2.a) Implement AND, OR, NOR by using NAND gates only.
b) Derive the hamming code for the sequence (101011). [5+5]

OR

3.a) Convert the following to the corresponding bases
i) $(343)_5$ = ( )$_6$
ii) $(7654)_8$ = ( )$_{10}$
b) Explain about even and odd parity check with an example, what is the drawback. [5+5]

4.a) Derive the sum of minterms for f(a,b,c,d)=a′b+ab′d+c′d
b) Derive and Implement Exclusive OR function involving three variables using only NAND function. [5+5]

OR

5.a) Obtain the simplified expression in POS (product of sums) of F(w,x,y,z)=π(1,2,4,7,12,14,15) using K-maps.
b) Implement the function f(a,b,c)=∑(1,3,4,6) using NOR-NOR two level gate structure. [5+5]

6. Realize a full subtractor using decoders. [10]

OR

7.a) Define a multiplexer? Draw a 2:1 multiplexer for the function f(x,y,z)=∑(0,2,3,5,7)
b) Write the steps involved in designing a combinational circuit. [5+5]

8. What is the drawback of JK flip flop, design a flip flop which overcomes this drawback and explain with neat diagram. [10]

OR

9.a) Draw the block diagram of asynchronous sequential circuit.

b) Analyze latch with NOR gates, derive transition, flow and state tables. [4+6]

10. Give the logic implementation of a 32 × 4 bit ROM using decoder of a suitable size. [10]

OR

11. What do you mean by register transfer? Explain in detail. Also discuss Three state bus buffer. [10]

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PART- A

(25 Marks)

1.a) Convert $(10110)_2$ to Gray code and $(110101)_G$ to binary number. [2]
b) Explain about Floating point number representation with an example. [3]
c) What are universal gates and why they are called as universal gates. [2]
d) Realize the following function as multilevel NAND-NAND network
$f = B(A + CD) + A\bar{C}$ [3]
e) What is a multiplexer? What is the function of a multiplexer's select input. [2]
f) Can more than one decoder output be activated at one time? Justify your answer? [3]
g) What is a flip-flop? Write down the characteristic equation of S-R flipflop. [2]
h) Discuss the difference between synchronous and asynchronous sequential circuits. [3]
i) What are shift micro operations and what are the different types. [2]
j) Explain about sequential programmable logic devices [3]

PART-B

(50 Marks)

2.a) Convert the following
i) $(53.625)_{10}$ to (? $)_2$ ii) $(3FD)_{16}$ to (? $)_2$ iii) $(A69.8)_{16}$ to (? $)_{10}$
b) Perform the decimal subtraction in 8-4-2-1 BCD using 9's complement
i) Subtract 79 from 26 ii) Subtract 748 from 983. [5+5]

OR

3.a) Simplify the following expression using Boolean algebra rules $\overline{\overline{A\bar{B} + ABC} + A(B + A\bar{B})}$
b) Check whether the received code 10101100 is correctly received or not if even parity is used. [5+5]

4.a) Reduce the following function using K-Map.
F(A,B,C,D,E) = Σm(1,4,8,10,11,20,22,24,25,26)+d(0,12,16,17)
b) Write down the procedure to convert a given AND-OR gate network to all NAND gate network and illustrate with an example. [5+5]

OR

5.a) Obtain the minimal sum of products expression for the following function and implement the same using only NAND gates
$f(A, B, C, D) = \sum(1,4,7,8,9,11) + \Sigma_d(0,3,5)$
b) Realize the following function with i) Multilevel NAND-NAND network and
ii) Multilevel NOR-NOR network.
$Y = \bar{A}B + B(C + D) + E\bar{F}(\bar{B} + \bar{D})$ [5+5]

6.a) What is a combinational logic circuit? Implement a Full adder using two half adders and one OR gate.

b) With a neat diagram explain in detail about Decimal Adder. [5+5]

OR

7.a) Design and explain a 4-bit binary parallel Adder/Subtractor.

b) Draw the logic diagram of 2:4 Decoder with an ENABLE input using: i) NAND gates ii) NOR gates. Show that the realization using NAND gates is more convenient to distinguish the selected output with a value of 0. [5+5]

8.a) Convert an SR Flip-Flop into JK Flip-Flop.

b) With a neat diagram explain about 4-bit bidirectional shift register. [5+5]

OR

9. Design the counter that goes through states 1,2,4,5,7,8,,10,11,1.....using JK flip-flops. [10]

10.a) A combinational circuit is defined by the functions:

$F_1 = \sum m(3,5,7)$ $F_2 = \sum m(4,5,7)$

Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs.

b) Explain about Read and Write cycles of a static RAM with neat timing waveforms. [5+5]

OR

11. With a neat diagram explain in detail about two dimensional memory decoding scheme. [10]

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